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UNITED STATES PATENT AND TRADEMARK OFFICE

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2. That I am well acquainted with the German and English languages.

3. That the attached is, to the best of my knowledge and belief, a true translation into the English language of the specification in German filed with the application for a patent in the U.S.A. on March 26, 2003
under the number 60/457,812.

4. That I believe that all statements made herein of my own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application in the United States of America or any patent issuing thereon.

For and on behalf of RWS Group plc

The 21st day of August 2003

S2357

Timing Recovery with free-running sampler, algorithmic phase detection and interpolation

Inventor: Peter Gregorius, COM ON CE

1. What technical problem is your invention intended to solve?

Recovery of data pulses which have been subjected to severe noise through a transmission line/channel. Band limiting of the transmission channel results in the signal being distorted by intersymbol interference at the receiver. The signal itself contains both deterministic and stochastic edge noise.

Particular requirements:

- Reliable recovery of the data in a very noisy environment.
- Multichannel application (Multiple Lane Application).
- Error rate BER<10^{-15}
- Small eye opening

2. How has this problem been solved until now? What disadvantages were associated with this?

The requirements on transceiver modules for speed, a low error rate (bit error rate, BER) and range for high-speed data transmission are becoming more stringent. It must be possible to transmit data in the Gigahertz band, for example at 2.488Gbits/s to 10Gbits/s, as far as possible without any errors, depending on the channel or transmission medium.

The arrangements for data recovery within the transceiver modules are referred to as *clock and data recovery* (CDR). There are essentially two fundamental concepts here: *phase alignment* and *phase picking*.

In the case of phase alignment, a phase locked loop is used to adjust the sampling time to the center of the eye of the received signal (bit cell). An edge-controlled D flipflop is generally used for recovery and synchronization, and for sampling the data at the D input with the rising edge at the clock input.

In the case of *phase picking*, to describe it in simplified form, the input signal is oversampled by connecting two or more D flipflops in parallel, with these D flipflops being clocked with stepped clock phases. For data recovery, a control circuit then selects the output of that D flipflop whose clock phase represents the optimum sampling time in the eye center.

Both methods may be carried out in many ways. In this case, multiphase circuits or phase locked loops of various configurations allow both the phase alignment method and the phase picking method to be implemented. At this point, reference should be made by way of example to two references [1] and [2]. These cited references admittedly do not reflect the latest current prior art, but are fundamental to the methods mentioned. All more recent publications are in general based on the methods that have been mentioned, but generally represent only a further development of the implementation in modern semiconductor processes.

Both methods require a phase detector, which assesses the phase angle of the input signal with respect to the clock phase or phases within the CDR. In this context, the prior art is essentially based on digital methods, see references [3]-[5], since these can be implemented more easily with analog methods. In abstracted form, a digital phase detector such as this may be regarded as an edge-controlled switching mechanism to which the received signal is supplied on the one hand and a clock phase is supplied on the other hand, and which detects the phase angle by internal state transitions. The

fundamental disadvantage of such digital phase detectors is that the received signal is subject to distortion and disturbances from various unavoidable effects in the transmission channel, such as reflection, attenuation, channel crosstalk and intersymbol interference.

Disadvantages of the conventional methods:

In the case of digital phase detectors, in which the received signal acts directly on edge-sensitive inputs, these disturbances generally lead to incorrect assessments of the phase angle. Although a very inert control system can be used to adequately suppress these incorrect assessments, provided that they do not occur excessively frequently, so that the disturbances do not immediately lead to unlocking of the phase locked loop, an incorrect assessment of the phase angle even with an inert control system in fact reduces the jitter budget, so that a greater eye opening is required for the received signal for the same bit error rate than would be the case for a phase detector that was less susceptible to disturbances. A further disadvantage is that the more inert control system results in the phase locked loop stabilization time becoming longer.

The data detection (recovery) is carried out at the data rate in conventional methods. The control loop for the phase alignment need not achieve the BER<10^{-15}, but the regenerative flipflop must have adequate stability. Metastability of the flipflop leads to incorrect decisions during data recovery.

In order to avoid these disadvantages, it is known for the phase information not to be obtained directly from the input signal, but for the received signal to be oversampled or for the phase angle to be derived from the sampled received signal. This is, of course, the normal method for phase picking CDRs.

Mixed signal control loops are generally relatively complex in their implementation. In order to guarantee the stability of the loop, additional circuit complexity is generally required. A solution which contains the control loop in only one domain will be advantageous.

3. How does your invention solve this problem, and what advantages does this solution offer?

Timing recovery is based on a free-running, analog sampling unit (sampler) followed by a demultiplexer. The serial data stream is converted to parallel form, and is thus transformed to a lower processing frequency. In order to obtain sufficiently accurate phase information, additional sample values are interpolated between the sample points. The degree of interpolation M depends on the desired phase resolution.

The advantage is the reduced analog circuit complexity and the maximum possible flexibility of the digital evaluation and control unit.

Furthermore, with a suitable implementation, it is possible to use the additional information relating to frequency errors from the digital control unit to control a digital PLL. The advantage of this solution is that the frequency of the analog sampling unit is readjusted at the same time. In order to avoid a closed control loop between the analog front end and the digital control unit, the control word for frequency correction can be transferred via a buffer store (FIFO).

Basic operation:

4. What is the essence of your invention?

A combination of discrete-time and continuous-time methods for data recovery based on phase interpolation. An algorithmic method is used for evaluation of the sampled signals. All the signal evaluation and processing is carried out using digital methods. The data recovery is implemented by an asymmetric form filter. The method is best suited to additional frequency correction without the necessity for a closed control loop from the timing recovery to the digital PLL.

5. Exemplary embodiment and/or implementation

See Figures 1-7

6. What steps are required to verify your invention in a competitor product?

Product analysis and measurements.

8. Literature

[1] IEEE JSSC, December 1992, Pages 1736-1746
Thomas Lee: "A 155-MHz Clock Recovery Delay and Phase Locked Loop"

[2] IEEE JSSC, December 1990, Pages 1385-1394
Paul R. Gray: "A 30-MHz Hybrid Analog/Digital Clock Recovery in 2-µm CMOS"

[3] Electronics Letter, October 1975, Pages 541-542
J.D.H. Alexander: "Clock Recovery from Random Binary Signals"

[4] IEEE, Journal of Lightwave Technology, December 1985, Pages 1312-1314
Ch. Hogge: "A Self Correcting Clock Recovery Circuit"

[5] ISCAS 2001, M. Ramezani and A. Salama: "An Improved Bang-Bang Phase Detector for Clock and Data Recovery Applications"

[6] C.W. Hangelsdorf, "A 400MHz Input Flash Counter with Correction",
IEEE Journal of Solid-State Circuits. Vol. 25, February 1990, pp. 184

[7] B. Engl/P. Gregorius, "Schaltungsanordnung zur Takt- und Datenrückgewinnung aus einem Empfangssignal", [Circuit arrangement for clock and data recovery from a received signal], 2001E17112DE